

ABSTRACT

A flash EPROM array (100) and method of manufacture is disclosed. Source regions (118a-118f) are shared between the memory cells (108a,l-108d,n) of row (104a-104d) pairs, and are isolated from one another in the row direction by isolation regions 120. Low resistance source conductor members (122a-122b) extend in the row direction and are formed over the source regions (118a-118f) and make contact therewith in a self-aligned fashion. The architecture allows for source decoding and thus enables user programmable sector erase architecture.



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